REMARKS

Applicant thanks Examiner for the detailed review of the application.

Claim Rejections -35 USC § 103(a)

The Office Action has rejected Claims 1, 3-6, 10, 14, and 16-20 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,195,728 to Bordaz et al. (referred to hereinafter as "Bordaz") in view of US. 6,134,631 to Jennings et al. (herein referred to as "Jennings").

"The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). The Office Action has failed to meet one or more of these requirements.

Applicant's amended claim 1 includes, "wherein the shared cache is to generate a first message to invalidate the block in a second processor core of the plurality of processor cores and provide a write acknowledgement to a requesting processor core." Note that neither Bordaz or Jennings discloses **a single message** capable of invalidating a block in one processor core, i.e. the second processor core, and providing a write acknowledgement to another core, i.e. a requesting core.

Applicant's claim 14 includes, "wherein the shared memory is to generate an evict message referencing an address to an owning processor core of the plurality of cores in response to receiving a read request referencing the address from a requesting core of the plurality of cores and the owning processor core owning a block associated with the address." Applicant respectfully submits that neither Bordaz and Jenning disclose generating an evict message to an owning core for a block when a read request referencing the block is received from another core.

Applicant's claim 18 includes, "capable of being held in a not present state, a present and owned by a core of the plurality of cores state, a present, not owned, and a core of the plurality of cores is a custodian state, and a present, not owned, and no core of the plurality of cores is a custodian state." The Office Action states that Bordaz discloses tag information to indicate if data is valid and if it is held exclusively. However, Bordaz does not disclose a cache line or block being capable of being held in all of the four listed states in claim 18. Furthermore, Bordaz does not disclose the notion of a custodian versus an owner, as illustrated in the disclosed state. Additionally, in reference to claim 20, neither Bordaz or Jennings, disclose a single message capable of invalidating all cores other than a requesting core in response to one of the listed states, i.e. present, not owned, and no core is a custodian, state.

Therefore, applicant respectfully request that independent claims 1, 14, and 18, as well as their currently pending dependent claims, are now in condition for allowance for at least the reasons

stated above.

If there are any additional charges, please charge Deposit Account No. 50-0221. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact David P. McAbee at (503) 712-4988.

Respectfully submitted,
Intel Corporation

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